WHAT IS CLAIMED IS:

1   1.   A MPEG decoder having a controller that detects start
2   codes in bitstreams received in said MPEG decoder, each of said
3   start codes having a three-byte start code prefix and a one-byte
4   start code value, said controller operable to (i) fetch a thirty-
5   two bit word of a received bitstream, (ii) determine whether a
6   start code prefix and a start code value are properly aligned
7   within said thirty-two bit word, and (iii) if not properly aligned
8   within said thirty-two bit word, determine whether the least
9   significant byte of said thirty-two bit word may be part of said
10   start code prefix.

1   2.   The MPEG decoder as set forth in Claim 1 wherein said
2   controller is further operable, if not part of said start code
3   prefix, to fetch another thirty-two bit word of said received
4   bitstream.

1   3.   The MPEG decoder as set forth in Claim 2 wherein said
2   controller is further operable to (iv) determine whether said start
3   code prefix is within the three least significant bytes of said
4   thirty-two bit word.

1   4.   The MPEG decoder as set forth in Claim 2 wherein said

2   controller is further operable to (iv) determine whether part of

3   said start code prefix may be within the most significant byte of

4   a next thirty-two bit word.

1   5.   The MPEG decoder as set forth in Claim 4 wherein said

2   controller is further operable to fetch said next thirty-two bit

3   word of said received bitstream.

1   6.   The MPEG decoder as set forth in Claim 4 wherein said

2   controller is further operable to (v) determine whether part of

3   said start code prefix is within the two least significant bytes of

4   said thirty-two bit word and the most significant byte of said next

5   thirty-two bit word.

1   7.   The MPEG decoder as set forth in Claim 4 wherein said

2   controller is further operable to (v) determine whether part of

3   said start code prefix is within the least significant byte of said

4   thirty-two bit word and the two most significant bytes of said next

5   thirty-two bit word.

1   8.   A digital video recorder capable of playing back a

2   recorded program stream, said digital video recorder comprising:

3   a video processor capable of receiving an incoming

4   program stream and converting said incoming program stream to a

5   baseband signal capable of being displayed on a television

6   associated with said digital video recorder;

7   a storage disk capable of storing program streams for

8   time-shifted viewing; and

9   a MPEG decoder capable of decoding received bitstreams

10   and generating PES packets, said MPEG decoder having a controller

11   that detects start codes in said received bitstreams, each of said

12   start codes having a three-byte start code prefix and a one-byte

13   start code value, said controller operable to (i) fetch a thirty-

14   two bit word of a received bitstream, (ii) determine whether a

15   start code prefix and a start code value are properly aligned

16   within said thirty-two bit word, and (iii) if not properly aligned

17   within said thirty-two bit word, determine whether the least

18   significant byte of said thirty-two bit word may be part of said

19   start code prefix.

1   9.   The digital video recorder as set forth in Claim 8

2   wherein said controller is further operable, if not part of said

3   start code prefix, to fetch another thirty-two bit word of said

4   recorded bitstream.

1   10. The digital video recorder as set forth in Claim 9

2   wherein said controller is further operable to (iv) determine

3   whether said start code prefix is within the three least

4   significant bytes of said thirty-two bit word.

1   11. The digital video recorder as set forth in Claim 9

2   wherein said controller is further operable to (iv) determine

3   whether part of said start code prefix may be within the most

4   significant byte of a next thirty-two bit word.

1   12. The digital video recorder as set forth in Claim 11

2   wherein said controller is further operable to fetch said next

3   thirty-two bit word of said received bitstream.

1   13. The digital video recorder as set forth in Claim 11

2 wherein said controller is further operable to (v) determine

3 whether part of said start code prefix is within the two least

4 significant bytes of said thirty-two bit word and the most

5 significant byte of said next thirty-two bit word.

1   14. The digital video recorder as set forth in Claim 11

2 wherein said controller is further operable to (v) determine

3 whether part of said start code prefix is within the least

4 significant byte of said thirty-two bit word and the two most

5 significant bytes of said next thirty-two bit word.

1   15.   A method of detecting start codes in bitstreams received

2   in a MPEG decoder, each of said start codes having a three-byte

3   start code prefix and a one-byte start code value, said method

4   comprising the steps of:

5   (i) fetching a thirty-two bit word of a received

6   bitstream;

7   (ii) determining whether a start code prefix and a start

8   code value are properly aligned within said thirty-two bit word;

9   and

10   (iii) if not properly aligned within said thirty-two bit

11   word, determining whether the least significant byte of said

12   thirty-two bit word may be part of said start code prefix.

1   16.   The method as set forth in Claim 15 further comprising

2   the step of (iv) determining whether said start code prefix is

3   within the three least significant bytes of said thirty-two bit

4   word.

1   17.   The method as set forth in Claim 15 further comprising

2   the step of (iv) determining whether part of said start code prefix

3   may be within the most significant byte of a next thirty-two bit

4   word.

1   18.   The method as set forth in Claim 17 further comprising

2   the step of fetching said next thirty-two bit word of said received

3   bitstream.

1   19.   The method as set forth in Claim 15 further comprising

2   the step of (v) determining whether part of said start code prefix

3   is within the two least significant bytes of said thirty-two bit

4   word and the most significant byte of a next thirty-two bit word.

1   20.   The method as set forth in Claim 15 further comprising

2   the step of (v) determining whether part of said start code prefix

3   is within the least significant byte of said thirty-two bit word

4   and the two most significant bytes of a next thirty-two bit word.